#15/10-11-01
V. Jones

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	DANIEL L. AUCLAIR, JEFFREY CRAIG, JOHN S. MANGAN, ROBERT D. NORMAN, DANIEL C. GUTERMAN and SANJAY MEHROTRA		
Title:	Soft Errors Handling in EEprom Devices		
Serial No.:	08/908,265	Filing Date:	August 7, 1997
Examiner:	E. Moise	Group Art Unit:	2133
Docket No.:	M-10202-3C US		

San Francisco, California
October 2, 2001

BOX AMENDMENT
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

RESPONSE TO OFFICE ACTION

Dear Sir:

These remarks are in response to the to the Official Action mailed on July 2, 2001. These claims had previously been indicated as allowable in the previous Office Action of October 24, 2000, that suspended prosecution due to the request for declaration of an interference. The present Office Action rejected claims 35-36 and 38-40 under 35 U.S.C., first paragraph. For the reasons given below, it respectfully submitted the present application provides support for the pending claims and that the rejection is consequently not well founded.

More specifically, the present Office Action states that it fails to find support for the last clause of claim 35, namely

> means for determining a likelihood that the memory device has a degraded state by applying each of a plurality of read voltages to a terminal of a first cell of the plurality of memory cells to generate a plurality of read results.

As noted in the Amendment and Request for Declaration of Interference, the present application has more than one embodiment of this invention which are used in differing embodiments. The following discussion begins by providing the support for the process of "applying each of a plurality of read voltages to a terminal of a first cell of the plurality of

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

3 EMBARCADERO CENTER
28TH FLOOR
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

memory cells to generate a plurality of read results" in different embodiments, followed by a discussion of the means used implement these processes.

Figure 8 of the present application is a flow chart of an embodiment for performing a program operation. This operation includes a "margining operation" which is an embodiment for the process of "determining a likelihood..." and "applying each of a plurality of voltages...". This figure is described mainly between page 23, line 6, and page 24, line 26, of the present application.

The margining operation is described on page 24, lines 5-23. Specifically, beginning on line 6, this section states:

> The read margining operation are subdivided into two sub-operations 804 and 806. In the first sub-operations [804], the control gate voltage is set to V_{PRH} ...and the data is read and compared with the actual data (as described above). ... In the second sub-operation [806], a voltage V_{PRL} ... is used. ... [I]f one of the two sub-operations fails (steps 805 and 807), the defect management operation will be performed.

Thus it is respectfully submitted that support is supplied for "determining a likelihood that the memory device has a degraded state [if NO in step 805 or 807] by applying each of a plurality of read voltages [V_{PRH} and V_{PRL}] to a terminal [control gate] of a first cell of the plurality of memory cells to generate a plurality of read results [steps 804, 805 and steps 806, 807]."

As for the "means for" executing this process, in the embodiment for a margining operation, this can be taken as the read READ CIRCUIT 213 and COMPARE CIRCUIT 217 of Figure 4. The elements are described on page 16, lines 10-24. Detail of the sensing operations is given with respect to Figures 6a and 6b beginning on page 18, line 18, with the use of the different control gate voltages for different ones of the reading processes presented on page 19, lines 19-27.

Figure 9 of the present application is a flow chart of an embodiment for performing a "scrub" operation which is an alternate embodiment for the process of "determining a likelihood..." and "applying each of a plurality of voltages...". This figure is described mainly between page 24, line 24, and page 26, line 3, of the present application.

The scrub operation is described on page 24, line 9, to page 25, line 22. Specifically, beginning on line 32 of page 24, this section states:

> In step 901, a control gate voltage V_{SH} ... is applied. The cells are read in step 902 to see if there is any error as determined by the ECC [error correction code] check. ... In step 903, the scrub operation is performed again ... with a control gate voltage V_{SL}... . The cells are read in step 904 to see if

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

3 EMBARCADERO CENTER
28TH FLOOR
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

there is any error as determined by the ECC check. ... In the scrub operation, ...the test can be performed utilizing the ECC logic 416 of Fig. 5.

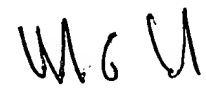
Thus it is respectfully submitted that support is supplied for "determining a likelihood that the memory device has a degraded state [if NO in step 902 or 904] by applying each of a plurality of read voltages [V_{SH} and V_{SL}] to a terminal [control gate] of a first cell of the plurality of memory cells to generate a plurality of read results [steps 901, 902 and steps 903, 904]."

As for the "means for" executing this process, in the embodiment for a scrub operation, this can be taken as the "ECC logic 416 of Fig. 5", as described in the quotation of the preceding paragraph. The operation of the ECC circuit is described on page 18, lines 7-17, with more detail given in the various applications incorporated into the present application by reference and listed beginning on page 22, line 35.

Therefore, for of any of these reasons, it is respectfully submitted that the present application fully supports the claimed subject matter, that a rejection under 35 U.S.C., first paragraph, is not well founded, and that claims 35-36 and 38-40 are allowable. Reconsideration of the Office Action's rejection of claims 35-36 and 38-40 and a prompt declaration of the requested interference is respectfully requested. In the meantime, however, if the Examiner has any questions about this request, application, or response, a telephone call to the undersigned is invited.

EXPRESS MAIL LABEL NO:
EL 896776943 US

Respectfully submitted,



Michael G. Cleveland
Attorney for Applicant(s)
Reg. No. 46,030

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

3 EMBARCADERO CENTER
28TH FLOOR
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646